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Code No. : 16349 N

**VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD**

Accredited by NAAC with A++ Grade

**B.E. (E.E.E.) VI-Semester Main Examinations, May/June-2023**

**Linear Integrated Circuits & Applications**

Time: 3 hours

Max. Marks: 60

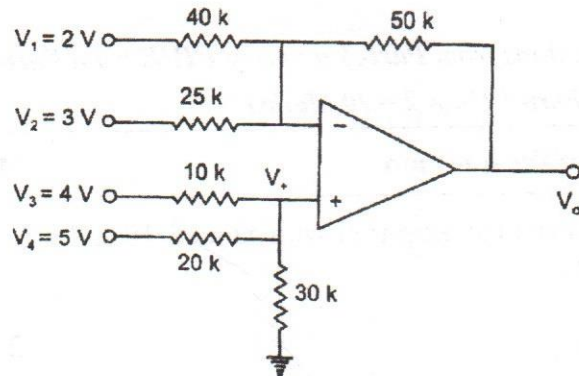
Note: Answer all questions from Part-A and any FIVE from Part-B

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Determine the feed back resistance of an amplifier with gain of -10 and input resistance equal to 10 kΩ.	2	3	1	1,2,3
2.	Define Slew rate of an op-amp.	2	1	1	1,2,3
3.	Describe the essential features of an instrumentation amplifier.	2	1	2	1,2,3
4.	Draw the circuit diagram of zero crossing detector using op-amp.	2	1	2	1,2,3
5.	What should be the amplifier gain for generating sustained oscillations in case of phase shift oscillator.	2	1	3	1,2,3
6.	Write the applications of Voltage Controlled Oscillator.	2	1	3	1,2,3
7.	Determine the output voltage for the regulator shown in figure.	2	3	4	1,2,3
8.	Distinguish between Pulse Width Modulation and Pulse Frequency Modulation.	2	2	4	1,2,3
9.	Which filter can act as phase corrector?	2	1	5	1,2,3
10.	Design a low pass filter at a cut off frequency of 1kHz with pass band gain of 2.	2	3	5	1,2,3

**Part-B (5 × 8 = 40 Marks)**

11. a) Find  $V_0$  for the adder-subtractor circuit shown in figure.



5    3    1    1,2,3

b) Discuss pole zero frequency compensation technique

3    2    1    1,2,3

12. a) With a neat circuit diagram, discuss the working of a positive clipper having reference voltage  $+V_{ref}$

4    2    2    1,2,3

b) Draw the circuit of a full wave rectifier using Op-Amp and explain its operation.

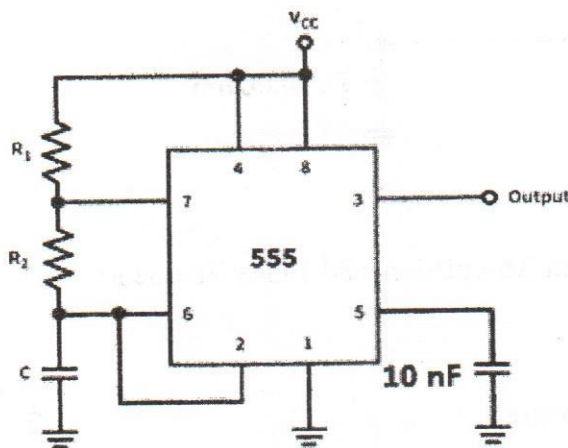
4    2    2    1,2,3

13. a) Discuss the monostable mode of operation of 555 timer with neat circuit diagram and waveforms.

4    2    3    1,2,3

b) In the Astable Multivibrator shown in figure  $R_1=2.2\text{ k}\Omega$ ,  $R_2=3.9\text{ k}\Omega$ , and  $C=0.1\text{ }\mu\text{F}$ . Determine the positive pulse width  $t_c$ , negative pulse width  $t_d$  and running frequency  $f_0$ .

4    3    3    1,2,3



14. a) Explain the operation of a shunt voltage regulator with a neat circuit diagram.

4    2    4    1,2,3



b)	Prove that using current foldback protection scheme short circuit current can be maintained at a value lower than rated current for voltage regulators.	4	3	4	1,2,3
15. a)	Explain the concept of switched capacitor filter and draw circuit configuration of realizing a Resistor.	4	2	5	1,2,3
b)	Design a wide band pass filter having $f_L=400$ Hz, $f_H=2$ kHz and pass band gain = 4.	4	3	5	1,2,3
16. a)	Draw the internal block diagram of an Op-Amp and explain the function of each stage.	4	1	1	1,2,3
b)	A Schmitt trigger with the upper threshold level $V_{UT}=0$ V and hysteresis width $V_H=0.2$ V converts a 1 kHz sine wave of amplitude 4Vpp into a square wave. Calculate the time duration of the negative and positive portion of the output wave form.	4	3	2	1,2,3
17.	Answer any <i>two</i> of the following:				
a)	With a neat block diagram explain the working of phase locked loop.	4	2	3	1,2,3
b)	Discuss the working of Buck switching regulator.	4	2	4	1,2,3
c)	Design a narrow band pass filter so that $f_c=1$ kHz $Q=3$ and $A_F=10$ .	4	3	5	1,2,3

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level - 1	21%
ii)	Blooms Taxonomy Level - 2	38.21%
iii)	Blooms Taxonomy Level - 3 & 4	40.79%

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